UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,021	11/14/2003	James C. Bartelo	FIS920030197US1	1020

29154 7590 06/07/2004

FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,021	BARTELO ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 - 22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 - 22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 November 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/14/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on November 14, 2003 was filed before the mailing date of the non-final rejection. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The specification is objected to because the top lines in every page are too close to top surface of the each page, making reading and entry of amendments difficult. Substitute specification with one and one-half line of extra margin at the top surface of each page on good quality paper is required.

Drawings

3. The drawings are objected to because the number of the figures and some numeral numbers in the figures (e.g., 6, 7 and 8) are not clearly written. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner

has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 - 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Andricacos et al. '320.

Regarding claims 1 and 12, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2, column 1, line 64 – column 2, line 4, column 4, lines 57 – 64, column 5, lines 38 – 48 and column 7, lines 1 – 10 an integrated circuit structure comprising:

- internal circuitry (active IC devices and circuits); and
- an interconnect (12, 16, 18, Cu cap layer and 20) on an external portion of said structure, said interconnect comprising:
    - a metal layer on a substrate (12; e.g., Al);
    - a first copper layer (16c; Cu) on said metal layer;
    - a barrier layer (18; e.g., Ni) on said copper layer;
    - a stabilizing copper layer (Cu cap layer; column 7, lines 1 - 4) on said barrier layer; and
    - a tin-based solder bump (20; e.g., eutectic PbSn alloy) on said barrier layer.

Regarding claims 2 and 13, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2, column 1, line 64 – column 2, line 4, column 4, lines 57 – 64, column 5, lines 38 – 48 and column 7, lines 1 – 10 said stabilizing copper layer comprising a "sufficient amount" of copper. Furthermore, since the structure recited in Andricacos et al. is same in structure to that of the claims, the following limitation "to balance the chemical potential gradient of copper across said barrier layer and prevent copper within said first copper layer from diffusing across said barrier layer" is inherent in Andricacos et al.

Regarding claims 3 and 14, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2, column 1, line 64 – column 2, line 4 and column 7, lines 1 – 10 the tin-based solder bump comprising a copper rich solder alloy (since the copper in the Cu cap layer dissolves in the Sn-based solder to form Cu/Sn intermetallics, the tin-based solder bump of Andricacos et al. read as a copper rich solder alloy).

Regarding claims 4, 9, 15 and 20, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2 and column 4, lines 57 – 64 said metal layer (12) comprising diffusion metallurgy including AI.

Regarding claims 5, 10, 16 and 21, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2 and column 5, lines 45 – 48 the barrier layer (18) comprising Ni.

Regarding claims 6, 11, 17 and 22, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2 and column 7, lines 8 – 10 said tin-based solder bump (20) comprising a eutectic PbSn solder.

Regarding claims 7 and 18, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2, column 1, line 64 – column 2, line 4, column 4, lines 57 – 64, column 5, lines 38 – 48 and column 7, lines 1 – 10 an integrated circuit structure comprising:

- internal circuitry (active IC devices and circuits); and

- an interconnect (12, 16, 18, Cu cap layer and 20) on an external portion of said structure, said interconnect comprising:
    - a metal layer on a substrate (12; e.g., Al);
    - a first copper layer (16c; Cu) on said metal layer;
    - a barrier layer (18; e.g., Ni) on said copper layer;
    - a copper and tin-based solder alloy bump (20; e.g., eutectic PbSn alloy with Cu that is dissolved from a Cu cap layer) on said barrier layer.

Regarding claims 8 and 19, Andricacos et al. discloses in e.g., Fig. 1, Fig. 2, column 1, line 64 – column 2, line 4, column 4, lines 57 – 64, column 5, lines 38 – 48 and column 7, lines 1 – 10 said copper and tin-based solder alloy bump comprising a "sufficient amount" of copper. Furthermore, since the structure recited in Andricacos et al. is same in structure to that of the claims, the following limitation "to balance the chemical potential gradient of copper across said barrier layer and prevent copper within said first copper layer from diffusing across said barrier layer" is inherent in Andricacos et al.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hwang et al. and Matsuki et al. disclose an interconnect structure for a solder ball.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
5/26/04 8:43:46 PM

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800